Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A structure of a substrate for a high-density semiconductor package comprising:
a metal substrate having a first surface and a second surface, wherein the first surface comprises at least a die attachment area located at a prescribed location;
an interconnect substrate having a top surface and a bottom surface, wherein said top surface of said interconnect substrate is attached to the second surface of the metal substrate, wherein said interconnect substrate comprises means for electrically connecting with the IC chip through one or more slots on the metal substrate with wire bonds, and wherein the bottom surface of the interconnect substrate comprises connection means for electrically connecting to a printed circuit board, so that signals from the IC chip can be transmitted through the interconnect substrate to a printed circuit board; and
at least a thermally conductive via attached to the second surface of the metal substrate underneath the die attachment area for connecting with the printed circuit board for conducting heat from the metal substrate to the printed circuit board.

[c2] 2. The structure according to claim 1, wherein the interconnect substrate comprises a plurality of wire bonding pads in prescribed locations, and wherein a laser beam is used to remove portions of the interconnect substrate to expose the wire bonding pads.

[c3] 3. The structure according to claim 2, wherein the exposed wire bonding pads is plated with Ni/Au metals.

[c4] 4. The structure according to claim 3, wherein the IC chip is electrically connected with the plated wire bonding pads using a plurality of bonding wires.

[c5] 5. The structure according to claim 3, wherein the Ni/Au plating step is performed after the last layer of metal is deposited and vias to the next to the last metal layer are connected.

[c6] 6. The structure according to claim 3, wherein the Ni/Au plating step is performed after the exposure of the wire bonding pads are completed by laser.

[c7] 7. The structure according to claim 3, wherein the Ni/Au plating step is performed before the last layer of metal is patterned so that in case there is an open line or open via in the preceding metal layers, the corresponding wire bonding pads will not have deposits of Ni/Au material on the pad surface so that deposits of Ni/Au material can be

visually inspected easily and therefore the need of an open test of a O/S test can be eliminated.

[c8] 8. The structure according to claim 1, wherein a plurality of thermal conductive vias and a plurality of signal/power conductive vias are disposed between the dielectric layers and on the bottom surface of the interconnect substrate for heat transfer and signal/power distribution respectively.

[c9] 9. The structure according to claim 1, wherein the metal panel is singulated into individual substrates to facilitate the IC chip attachment and other assembly steps.

[c10] 10. The structure according to claim 1, wherein the metal panel is comprised of a single strip or a plurality of strips having a plurality of die attachment areas, wherein each said die attachment area is to facilitate IC chip attachment and other assembly steps.

[c11] 11. The structure according to claim 1, wherein a material for making the metal substrate can be one selected from a group consisting of copper, stainless steel or aluminum.

[c12] 12. The structure according to claim 1, wherein more than one die attachment areas can be formed on the metal substrate, and wherein for each die attachment

area, one or more wire bonding slots are fabricated on the metal substrate for wire bonding.

[c13] 13. The structure according to claim 1, wherein the dielectric material is screened on the metal substrate or laminated on the metal panel as part of a build up process.

[c14] 14. The structure according to claim 1, wherein the dielectric material is comprises of a glass fiber material to strengthen the areas underneath the wire bond pads.

[c15] 15. The structure according to claim 1, wherein a metal foil is laminated on the metal substrate as part of a interconnect forming process.

[c16] 16. The structure according to claim 1, wherein a metal layer is formed directly on top of the dielectric film by performing a wet etching step.

[c17] 17. The structure according to claim 1, wherein one or more metal layers are formed using the thin film semi-additive plating process.

[c18] 18. The structure according to claim 1, wherein a sub-assembly of metal/dielectric layers is pre-fabricated in the interconnect substrate and then the interconnect substrate is attached to the metal panel as part of the

fabrication process.

[c19] 19. The structure according to claim 1, wherein a set of pedestals are etched or plated on the metal substrate surface at prescribed regions of the BGA pads before the dielectric layer is deposited, so that the dielectric layer thickness in the prescribed regions is reduced to substantially facilitate thermal vias to conduct heat to the BGA pads.

[c20] 20. The structure according to claim 1, wherein a plurality of pins are attached to the second surface of the interconnect substrate to make a pin grid array (PGA) substrate.

[c21] 21. The structure according to claim 1, wherein a plurality of hard gold pads are plated on the second surface of the interconnect substrate to make a land grid array (LGA) substrate.